4875 79846

SEARCH REQUEST FORM **Scientific and Technical Information Center - EIC2800**

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Date 11/8/02 Serial # 10/010,237 Priority Application Date 12/7/01

Your Name M. Lewis Examiner # _____

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In what format would you like your results? Paper is the default. (PAPER) DISK EMAIL

If submitting more than one search, please prioritize in order of need.

The EIC searcher normally will contact you before beginning a prior art search. If you would like to sit with a searcher for an interactive search, please notify one of the searchers.

Where have you searched so far on this case? 11-08-02 P04:19 IN

Circle: USPT DWPI EPO Abs JPO Abs IBM TDB

Other: _____

What relevant art have you found so far? Please attach pertinent citations or Information Disclosure Statements. _____

What types of references would you like? Please checkmark:

Primary Refs ___ Nonpatent Literature ___ Other _____

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What is the topic, such as the **novelty**, motivation, utility, or other specific facets defining the desired **focus** of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims.

Claims 1-17

Problem See Page 1 Paragraph 1-3
" 2 4 4

Solution " " " " 5-7
" Abstract

See structure illustrated in the

Staff Use Only		Type of Search		Vendors	
Searcher:	Bode Ramesh Kumar	Structure (#)		STN	
Searcher Phone:	605-1726	Bibliographic	✓	Dialog	✓
Searcher Location:	STIC-EIC2800, CP4-9C18	Litigation		Questel/Orbit	
Date Searcher Picked Up:	11-14-02	Fulltext	✓	Lexis-Nexis	
Date Completed:	11-15-02	Patent Family		WWW/Internet	
Searcher Prep/Rev Time:	60	Other		Other	IBM-TBB's
Online Time:	240				

Day : Thursday
Date: 11/14/2002

PALM INTRANET

Time: 15:18:52

Application Number Information

Application Number: **10/010237**
Assignments
Filing Date: **12/07/2001**
Effective Date: **12/07/2001**
Application Received: **12/10/2001**
Patent Number:
Issue Date: **00/00/0000**
Date of Abandonment: **00/00/0000**
Attorney Docket Number: **03226/092001**
Status: **30 /DOCKETED NEW CASE - READY FOR EXAMINATION**
Confirmation Number: **5837**
Title of Invention: **WINDOW FRAME CAPACITOR**

Examiner Number: **73172 / LEWIS, MONICA**
Group Art Unit: **2822**
Class/Subclass: **257/680.000**
Lost Case: **NO**
Interference Number:
Unmatched Petition: **NO**
L&R Code: Secrecy Code:**1**
Third Level Review: **NO**
Secrecy Order: **NO**
Status Date: **05/03/2002**

Bar Code	Location	Location Date	Chrg to Loc	Charge to Name	Emp. ID	Infra Loc
10010237	2800 TC-2800 PAPER MATCHING, CP4 10C18	10/08/2002	28X1	LEWIS, MONICA	YABEBECH	CP4/10/C 18

Appln Info | Contents | Petition Info | Atty/Agent Info | Continuity Data | Foreign Data

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Pre-Grant Publication Information

Application Number : **10/010237** Confirmation Number : **5837**

Non Pub. Req.: N **Non Pub. Rescind Req.**: N **Early Pub. Req.**: N

Filing Type	Status Description	Projected Pub. Date	Bio Ind	Pub. Status	Actual Pub. Date	Publication Number	Exported?
NEW	PPUB	06/12/2003	N	ELIGIBLE			N

US CLASSIFICATION

Classification No.	Sub-class No.	Primary Class
257	680000	Y

Appln Info | Contents | Petition Info | Atty/Agent Info | Continuity Data | Foreign

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Attorney Docket # [ ] Search

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Set      Items   Description
S1     1847172   SEMI()CONDUCTOR? OR SEMICONDUCTOR? OR WAFER? OR IC OR INTE-
             GRATED()CIRCUIT? OR SILICON(3N)SUBSTRAT?
S2       22313   (TOP OR UPPER OR LOWER OR BOTTOM)()SURFACE?
S3     3353012   APERTUR? OR ORIFICE OR OPENING? OR HOLE? OR GAP? ? OR SPAC-
             E? OR CAVIT? OR NOTCH
S4           2   (WINDOWFRAME? OR WINDOW()FRAM?)(3N)CAPACIT?
S5          26   S1 AND S2 AND S3 AND CAPACIT?
S6          21   RD (unique items)
S7          18   S6 AND PY<=2001
S8       80296   CAPACIT? AND (WINDOW? OR S3)
S9       12896   CAPACIT?(6N)(WINDOW? OR S3)
S10       5274   CAPACIT?(2N)(WINDOW? OR S3)
S11          2   S10 AND S2
S12          2   S11 NOT S7
?show files
File   2:INSPEC 1969-2002/Nov W2
         (c) 2002 Institution of Electrical Engineers
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         (c)2002 Japan Science and Tech Corp(JST)
File  99:Wilson Appl. Sci & Tech Abs 1983-2002/Sep
         (c) 2002 The HW Wilson Co.
File 144:Pascal 1973-2002/Nov W2
         (c) 2002 INIST/CNRS
File 305:Analytical Abstracts 1980-2002/Oct W4
         (c) 2002 Royal Soc Chemistry
File 315:ChemEng & Biotec Abs 1970-2002/Oct
         (c) 2002 DECHEMA
?
```

7/9,K/10 **(Item 10 from file: 2)**
DIALOG(R)File 2:INSPEC

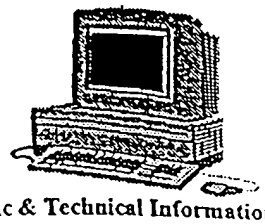
00816971 INSPEC Abstract Number: B75036631
Title: Contact device for testing semiconductor
Assignee(s): Philips Electronic Ind
Patent Number: GB 1385977 Issue Date: 750305
Application Date: 720516
Priority Appl. Number: NL 6853 Priority Appl. Date: 710519
Country of Publication: UK
Language: English Document Type: Patent (PT)
Treatment: Applications (A)
Abstract: A device for use in the electrical measurement of resistivity, sheet resistance, spreading resistance or **capacitance** has a block of insulating material whose **upper surface** is flat and supports a test body, the block including a duct with one end **opening** to the **upper surface** and the other end communicating with a reservoir for electrically conductive liquid, e.g. mercury, which reservoir communicates through a duct with a connection through which air under pressure is supplied to force the mercury into contact with the test body over an area defined by the cross-section of the duct at the **upper surface** , an electrical connection bolt contacting the mercury to provide an external connection to a measuring instrument. A contact pin may be spring-urged into electrical contact with the back of the disc.
Subfile: A B
Descriptors: electrical contacts; **semiconductor** materials testing; test equipment
Identifiers: duct; reservoir; electrically conductive liquid; mercury; electrical connection bolt; external connection; contact pin; contact device; **semiconductor** testing
Class Codes: A8170 (Materials testing); B0590 (Materials testing); B2180 (Electrical contacts); B2560 (Semiconductor devices)

Title: Contact device for testing semiconductor
Abstract: A device for use in the electrical measurement of resistivity, sheet resistance, spreading resistance or **capacitance** has a block of insulating material whose **upper surface** is flat and supports a test body, the block including a duct with one end **opening** to the **upper surface** and the other end communicating with a reservoir for electrically conductive liquid, e.g. mercury...

...test body over an area defined by the cross-section of the duct at the **upper surface** , an electrical connection bolt contacting the mercury to provide an external connection to a measuring...
...Descriptors: **semiconductor** materials testing
...Identifiers: **semiconductor** testing
1975
?

EIC2800

Search Results Feedback Form (Optional)



Scientific & Technical Information

The search results generated for your recent request are attached. If you have any questions or comm (compliments or complaints) about the scope or the results of the search, please contact *the EIC sear* who conducted the search *or contact*:

Jeff Harrison, Team Leader, 306-5429

Voluntary Results Feedback Form

- *I am an examiner in Workgroup:* _____ *(Example: 2830)*
- *Relevant prior art found, search results used as follows:*
  - ☐ 102 rejection
  - ☐ 103 rejection
  - ☐ Cited as being of interest.
  - ☐ Helped examiner better understand the invention.
  - ☐ Helped examiner better understand the state of the art in their technology.

Types of relevant prior art found:

- ☐ Foreign Patent(s)
- ☐ Non-Patent Literature
  (journal articles, conference proceedings, new product announcements etc.)

- *Relevant prior art not found*:
  - ☐ Results verified the lack of relevant prior art (helped determine patentability).
  - ☐ Search results were not useful in determining patentability or understanding the i

Other Comments:

Drop off completed forms in CP4-9C18, or send to Jeff Harrison, CP4-9C18.

To: Monica Lewis
From: Bode Fagbohunka
Subject: Online Search
Date:- November 15, 2002

Please find attached the results of your search for 10/010,237. The search was conducted using the standard collection of databases on dialog for EIC 2800. The tagged references appear to be the closest references located during our search.

If you would like a re-focus please let me know or if you have any questions regarding the search results please do not hesitate to contact me.

Bode Fagbohunka
703-605-1726

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Set      Items   Description
S1     1216925   SEMI()CONDUCTOR? OR SEMICONDUCTOR? OR WAFER? OR IC OR INTE-
             GRATED()CIRCUIT? OR SILICON(3N)SUBSTRAT?
S2      299167   (TOP OR UPPER OR LOWER OR BOTTOM)()SURFACE?
S3     3441890   APERTUR? OR ORIFICE OR OPENING? OR HOLE? OR GAP? ? OR SPAC-
             E? OR CAVIT? OR NOTCH
S4           1   (WINDOWFRAME? OR WINDOW()FRAM?)(3N)CAPACITOR?
S5         740   S1 AND S2 AND S3 AND CAPACITOR?
S6          10   S1(3N)S2(3N)S3(3N)CAPACITOR?
S7       31931   CAPACITOR? AND (WINDOW? OR S3)
S8        3416   CAPACITOR?(3N)(WINDOW? OR S3)
S9         265   CAPACITOR?(N)(WINDOW? OR S3)
S10         23   S9 AND S2
? show files
File 347:JAPIO Oct 1976-2002/Jun(Updated 021004)
         (c) 2002 JPO & JAPIO
File 350:Derwent WPIX 1963-2002/UD,UM &UP=200272
         (c) 2002  Thomson Derwent
?
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6/9,K/8 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013196830 **Image available**
WPI Acc No: 2000-368703/200032
XRPX Acc No: N00-276022

Socket board used for mounting integrated circuit during test, mounts chip capacitor vertically on undersurface and electrically connects capacitor terminals with that of semiconductor device via through-holes

Patent Assignee: ANDO ELECTRIC CO LTD (ANDN)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 11312766	A	19991109	JP 98119587	A	19980428	200032	B

Priority Applications (No Type Date): JP 98119587 A 19980428
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 11312766	A		5	H01L-023/32	

Abstract (Basic): JP 11312766 A

NOVELTY - Socket board (21) mounts **semiconductor** device (11) on the **upper surface** , vertically mounts the chip **capacitor** (7) on the under surface and has through- **holes** (6) connecting the terminals of the semiconductor device with the terminals of the chip capacitor.

USE - For mounting semiconductor IC such as BGA package during test.

ADVANTAGE - Enables to directly attach the chip component to arbitrary pins and to reduce the installation area of the chip component on the back side of the socket board. Eliminates the problem of covering the through-holes with the chip component and enables to reliably mount the chip component. Prevents damage of the chip capacitor by contacting with other components.

DESCRIPTION OF DRAWING(S) - The figure shows the schematic sectional view of the socket board.

Through-holes (6)
Chip capacitor (7)
Semiconductor device (11)
Socket board (21)
pp; 5 DwgNo 1/9

Title Terms: SOCKET; BOARD; MOUNT; INTEGRATE; CIRCUIT; TEST; MOUNT; CHIP; CAPACITOR; VERTICAL; UNDERSURFACE; ELECTRIC; CONNECT; CAPACITOR; TERMINAL; SEMICONDUCTOR; DEVICE; THROUGH; HOLE
Derwent Class: U11
International Patent Class (Main): H01L-023/32
International Patent Class (Additional): H01L-025/00
File Segment: EPI
Manual Codes (EPI/S-X): U11-C; U11-D01Q

Abstract (Basic):
... Socket board (21) mounts **semiconductor** device (11) on the **upper surface** , vertically mounts the chip **capacitor** (7) on the under surface and has through- **holes** (6) connecting the terminals of the semiconductor device with the terminals of the chip capacitor.

?

6/9,K/7 **(Item 4 from file: 350)**

013266005 **Image available**
WPI Acc No: 2000-437910/200038
XRPX Acc No: N00-327812

Concave capacitor **manufacture for e.g. dynamic RAM, involves enclosing** upper surface **and jointing** spacer **of** semiconductor **substrate exposed by storage node** hole **of concave pattern after patterning process**

Patent Assignee: SAMSUNG ELECTRONICS CO LTD (SMSU)
Inventor: LEE B T; LIM H J; LEE B; LIM H
Number of Countries: 004 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2000156483	A	20000606	JP 99198014	A	19990712	200038	B
KR 2000032886	A	20000615	KR 9849503	A	19981118	200110	
TW 426994	A	20010321	TW 99105639	A	19990409	200151	
US 6284589	B1	20010904	US 99392906	A	19990909	200154	
KR 275752	B	20001215	KR 9849503	A	19981118	200175	

Priority Applications (No Type Date): KR 9849503 A 19981118
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2000156483	A		8	H01L-027/108	
KR 2000032886	A			H01L-027/108	
TW 426994	A			H01L-027/10	
US 6284589	B1			H01L-021/8242	
KR 275752	B			H01L-027/108	Previous Publ. patent KR 2000032886

Abstract (Basic): JP 2000156483 A

NOVELTY - The patterning of a layer insulation film (20) on a semiconductor substrate (10) is performed to form a concave pattern (38a) with a storage node hole. A lower part electrode (60a) encloses the upper surface and jointing spacer (50a) of the substrate exposed by the storage node hole of the concave pattern.

USE - For dynamic RAM.

ADVANTAGE - Improves bonding strength of lower part electrode and concave pattern to prevent degradation of electrical property of a capacitor even if the lower part electrode is lifted.

DESCRIPTION OF DRAWING(S) - The figure shows the sectional view for explaining the manufacturing process of concave capacitor.

Semiconductor substrate (10)
Layer insulation film (20)
Concave pattern (38a)
Jointing spacer (50a)
Lower part electrode (60a)
pp; 8 DwgNo 1/10

Title Terms: CONCAVE; CAPACITOR; MANUFACTURE; DYNAMIC; RAM; ENCLOSE; UPPER; SURFACE; JOINT; SPACE; SEMICONDUCTOR; SUBSTRATE; EXPOSE; STORAGE; NODE; HOLE; CONCAVE; PATTERN; AFTER; PATTERN; PROCESS
Derwent Class: U11; U13
International Patent Class (Main): H01L-021/8242; H01L-027/10; H01L-027/108
International Patent Class (Additional): H01L-021/822; H01L-027/04
File Segment: EPI
Manual Codes (EPI/S-X): U11-C05G1B; U11-C18B5; U13-C04B1A; U13-D07

Concave capacitor **manufacture for e.g. dynamic RAM, involves enclosing** upper surface **and jointing** spacer **of** semiconductor **substrate exposed by storage node** hole **of concave pattern after patterning process**

6/9,K/6 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013292419 **Image available**
WPI Acc No: 2000-464354/200040
XRAM Acc No: C00-139849
XRPX Acc No: N00-346469

Semiconductor device manufacture uses a multi layer stack on the top surface of a semiconductor chip to form a capacitor that extends to the top of the surface of the chip

Patent Assignee: INFINEON TECHNOLOGIES NORTH AMERICA CORP (SIEI)
Inventor: KUNKEL G; LIAN J

Number of Countries: 029 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6083788	A	20000704	US 99277669	A	19990326	200040	B
EP 1039535	A2	20000927	EP 2000104731	A	20000304	200048	
JP 2000323685	A	20001124	JP 200087033	A	20000327	200064	
CN 1272687	A	20001108	CN 2000104816	A	20000327	200114	
KR 2000076953	A	20001226	KR 200015089	A	20000324	200134	

Priority Applications (No Type Date): US 99277669 A 19990326
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6083788	A		8	H01L-021/8242	
EP 1039535	A2	E		H01L-021/8242	
	Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI				
JP 2000323685	A		24	H01L-027/108	
CN 1272687	A			H01L-021/70	
KR 2000076953	A			H01L-027/108	

Abstract (Basic): US 6083788 A

NOVELTY - Manufacture of a semiconductor device comprises forming a connection, which is free of a diffusion barrier, between a conductive plug that overlies the source/drain region of the transistor and a metal bottom electrode of the capacitor. The bottom electrode is partially offset from the conductive polysilicon plug.

DETAILED DESCRIPTION - Manufacture of a **semiconductor** device comprises preparing a **silicon substrate** having a **top surface** (26) with **spaced** apart doped silicon regions. A separate stacked **capacitor** is serially connected to each silicon region. A first dielectric layer (14), a separate conductive plug (12) extending vertically through the layer to contact one of the regions, a dielectric third layer (16), and a conductive fourth layer, are formed. The conductive fourth layer is patterned to leave over the dielectric third layer, conductive segments (20), one for each conductive plug in partially offset alignment with the conductive plug, each suitable for serving as the bottom electrode of a stacked capacitor. A dielectric fifth layer (22) is formed over the resulting stack including the conductive segments. A conductive sixth layer (24) and a planarized dielectric seventh layer is also formed over the resulting stack. The seventh (25), sixth, fifth, and third layers are patterned to form in the stack separate openings, each exposing the top portion of a conductive plug that is not underlying a segment of the conductive fourth layer. A conductive material is provided in each separate opening for connecting the exposed top portion of each conductive plug selectively to a separate segment of the conductive layer. An INDEPENDENT CLAIM is also included for a memory cell including a transistor in a semiconductive chip and a stacked capacitor over a top surface of the semiconductive chip in which the bottom electrode of the stacked capacitor is a metal layer that makes a low resistance connection to a source/drain region of the transistor. The connection is free of a diffusion barrier and is made between a conductive plug that overlies the source/drain region of the transistor and a metal bottom electrode of the capacitor. The bottom electrode of the capacitor is partially offset from the conductive polysilicon plug.

USE - For the manufacture of a semiconductor device.

ADVANTAGE - Avoids need for the diffusion barrier between the capacitor electrode and the conductive plug, and any further heating to high temperatures in an oxygen-containing atmosphere that might affect the interface between the platinum and the silicon.

DESCRIPTION OF DRAWING(S) - The drawing shows the formation of a connection between a polysilicon plug and the bottom electrode of a stacked capacitor.

conductive plug (12)
first dielectric layer (14)
dielectric third layer (16)
conductive segments (20)
dielectric fifth layer (22)
conductive sixth layer (24)
dielectric seventh layer (25)
top surface (26)
pp; 8 DwgNo 9/9

Technology Focus:

TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Materials: The conductive plug is tungsten, aluminum, titanium nitride, or preferably doped polysilicon. The conductive fourth layer is iridium, palladium, ruthenium, silver, or preferably platinum. The conductive material provided in each separate opening is doped polysilicon. The dielectric fifth layer is lead zirconium titanate, strontium bismuth tantalate, barium titanate, or preferably barium strontium titanate.

Title Terms: SEMICONDUCTOR; DEVICE; MANUFACTURE; MULTI; LAYER; STACK; TOP; SURFACE; SEMICONDUCTOR; CHIP; FORM; CAPACITOR; EXTEND; TOP; SURFACE; CHIP

Derwent Class: L03; U12; U14

International Patent Class (Main): H01L-021/70; H01L-021/8242; H01L-027/108

International Patent Class (Additional): H01L-021/02; H01L-021/8239; H01L-027/10

File Segment: CPI; EPI

Manual Codes (CPI/A-N): L03-G04A; L04-C02; L04-C06; L04-C11C; L04-C12; L04-C14A; L04-E01

Manual Codes (EPI/S-X): U12-C02A1; U14-A03B4

Abstract (Basic):

... Manufacture of a **semiconductor** device comprises preparing a **silicon substrate** having a **top surface** (26) with **spaced** apart doped silicon regions. A separate stacked **capacitor** is serially connected to each silicon region. A first dielectric layer (14), a separate conductive...

10/5,K/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

06309952 **Image available**
FABRICATION OF SEMICONDUCTOR ELEMENT

PUB. NO.: 11-251550 [JP 11251550 A]
PUBLISHED: September 17, 1999 (19990917)
INVENTOR(s): ZURCHER PETER
JONES ROBERT E JR
MANIAR PAPU D
PEA CHU
APPLICANT(s): MOTOROLA INC
APPL. NO.: 10-351720 [JP 98351720]
FILED: December 10, 1998 (19981210)
PRIORITY: 995534 [US 995534], US (United States of America), December 22, 1997 (19971222)
22756 [US 22756], US (United States of America), February 12, 1998 (19980212)
INTL CLASS: H01L-027/108; H01L-021/8242

ABSTRACT

PROBLEM TO BE SOLVED: To fabricate high density bit cell capacitors by depositing a capacitor dielectric layer on the exposed first capacitor electrode layer and dielectric layer, depositing a second capacitor electrode layer entirely thereon and patterning to form a second capacitor electrode.

SOLUTION: A first dielectric layer 206 is deposited on a substrate 200 and a first **capacitor cavity** is formed therein. A first capacitor electrode layer 210 is deposited entirely on the **upper surface** of the first dielectric layer 206 and the first **capacitor cavity** and subjected to mechanochemical polishing to expose the **upper surface** of the first dielectric layer 206 before a first capacitor electrode is formed in the first **capacitor cavity** . A capacitor dielectric layer 242 and a second capacitor electrode layer 244 are then deposited sequentially on the exposed first capacitor electrode 210 and the dielectric layer 206 and patterned to form a second capacitor electrode.

ABSTRACT

... SOLUTION: A first dielectric layer 206 is deposited on a substrate 200 and a first **capacitor cavity** is formed therein. A first capacitor electrode layer 210 is deposited entirely on the **upper surface** of the first dielectric layer 206 and the first **capacitor cavity** and subjected to mechanochemical polishing to expose the **upper surface** of the first dielectric layer 206 before a first capacitor electrode is formed in the first **capacitor cavity** . A capacitor dielectric layer 242 and a second capacitor electrode layer 244 are then deposited...

10/5,K/2 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

06309948 **Image available**
SEMICONDUCTOR STORAGE DEVICE AND ITS MANUFACTURE

PUB. NO.: 11-251546 [JP 11251546 A]
PUBLISHED: September 17, 1999 (19990917)
INVENTOR(s): YOSHIDA KIYOKO
OZAKI TORU
APPLICANT(s): TOSHIBA CORP
APPL. NO.: 10-047107 [JP 9847107]
FILED: February 27, 1998 (19980227)
INTL CLASS: H01L-027/108; H01L-021/8242

ABSTRACT

PROBLEM TO BE SOLVED: To provide a stacked DRAM of high accuracy as well as high density, and its manufacturing method.

SOLUTION: A plurality of gate electrodes 5 are formed in parallel with each other, by depositing an insulating film and a conductive material on a semiconductor substrate 1. An impurity diffused layer 6 is formed on an element forming region 3 of the surface part of the semiconductor substrate 1, isolated by an amount equivalent to the width of the gate electrodes 5. After an embedded electrode 16 has been formed, an interlayer insulating film 12 is deposited on the entire surface, and a plurality of bit line trenches 27 intersecting the gate electrodes 5 perpendicularly are formed in parallel with each other. A plurality of bit lines 8 having an interlayer insulating film 13 on the **upper surfaces** are formed by depositing a conductive material and an insulating film in order on the bit line trenches 27, the interlayer insulating film 12 is patterned by using the interlayer insulating film 13 as a mask, and **capacitor apertures** 28 are formed above the impurity diffused layer 6. An accumulation electrode 17 is formed by depositing a conductive material inside the **capacitor apertures** 28 in such a manner that the height of the upper end is made at most the height of the **upper surface** of the interlayer insulating film 13, and a capacitor insulating film 18 and an upper electrode 19 are formed successively.

ABSTRACT

... other. A plurality of bit lines 8 having an interlayer insulating film 13 on the **upper surfaces** are formed by depositing a conductive material and an insulating film in order on the...
... film 12 is patterned by using the interlayer insulating film 13 as a mask, and **capacitor apertures** 28 are formed above the impurity diffused layer 6. An accumulation electrode 17 is formed by depositing a conductive material inside the **capacitor apertures** 28 in such a manner that the height of the upper end is made at most the height of the **upper surface** of the interlayer insulating film 13, and a capacitor insulating film 18 and an upper...

10/5,K/5 (Item 2 from file: 350)

014253543 **Image available**
WPI Acc No: 2002-074243/200210
XRAM Acc No: C02-021957
XRPX Acc No: N02-054736

Fabrication of capacitor under bit line structure for dynamic random access memory device, involves forming transfer gate transistors, self-aligned contact openings, conductive plugs, capacitor openings **and bit line contact hole**

Patent Assignee: TAIWAN SEMICONDUCTOR MFG CO (TASE-N)
Inventor: TU K; YU C
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6300191	B1	20011009	US 2001783382	A	20010215	200210	B

Priority Applications (No Type Date): US 2001783382 A 20010215
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6300191	B1		13	H01L-021/8242	

Abstract (Basic): US 6300191 B1

NOVELTY - A capacitor under bit line structure is formed by subsequently providing transfer gate transistors on semiconductor substrate, self-aligned contact (SAC) openings to expose top portions of the source/drain regions, conductive plugs, **capacitor openings** to expose top portion of conductive plugs to be used for storage node

contacts, and a bit line contact hole.

DETAILED DESCRIPTION - Fabrication of capacitor under bit line structure (33) involves: forming transfer gate transistors on semiconductor substrate, self-aligned contact (SAC) openings in a first insulator layer to expose top portions of the source/drain regions, first and second conductive plugs (21c) in the SAC **openings** , **capacitor openings** in a second insulator layer to expose the top portion of a first group of conductive plugs to be used for storage node contacts, and a bit line contact hole to expose the second group of conductive plugs to be used as a lower level bit line contact structure (16); depositing a conductive layer, such as a first polysilicon layer, to cover exposed surfaces of the **capacitor openings** , thus completely filling the bit line contact hole with the first polysilicon layer; removing portions of the conductive layer from the **top surface** of the second insulator layer, to form storage node structures in the **capacitor openings** , and to form an upper level, bit line contact structure in the bit line contact hole; depositing a capacitor dielectric layer, a polysilicon layer, and an overlying third insulator layer; performing a patterning procedure in the third insulator layer, in the second polysilicon layer, and in the capacitor dielectric layer, to form a bit line opening to expose the **top surface** of the upper level bit line contact structure, and to define capacitor structures (29) consisting of an overlying top electrode structure comprised of the second polysilicon layer, the capacitor dielectric layer, and the storage node structure; forming second insulator spacers on the sides of the bit line opening; and forming a bit line structure in the bit line contact opening.

USE - The method is used for forming capacitor under bit line (CUB) for dynamic random access memory (DRAM) device.

ADVANTAGE - The method reduces aspect ratio of a dry etched bit line contact hole, and reduces the risk of leakage and shorts between a stacked capacitor structure and a bit line structure.

DESCRIPTION OF DRAWING(S) - The figure is a schematic cross-section of a CUB DRAM device produced by the above method.

Insulators (11, 17, 26)
Contact structure (16)
Conductive plugs (21c)
Capacitor structures (29)
Titanium layer (30)
Titanium nitride layer (31)
Tungsten layer (32)
Bit line structure (33)
pp; 13 DwgNo 10/10

Title Terms: FABRICATE; CAPACITOR; BIT; LINE; STRUCTURE; DYNAMIC; RANDOM; ACCESS; MEMORY; DEVICE; FORMING; TRANSFER; GATE; TRANSISTOR; SELF; ALIGN; CONTACT; OPEN; CONDUCTING; PLUG; CAPACITOR; OPEN; BIT; LINE; CONTACT; HOLE

Derwent Class: L03; U11; U12; U14

International Patent Class (Main): H01L-021/8242

File Segment: CPI; EPI

... **random access memory device, involves forming transfer gate transistors, self-aligned contact openings, conductive plugs,** capacitor openings **and bit line contact hole**

Abstract (Basic):

... aligned contact (SAC) openings to expose top portions of the source/drain regions, conductive plugs, **capacitor openings** to expose top portion of conductive plugs to be used for storage node contacts, and...

... portions of the source/drain regions, first and second conductive plugs (21c) in the SAC **openings** , **capacitor openings** in a second insulator layer to expose the top portion of a first group of ...

...a conductive layer, such as a first polysilicon layer, to cover exposed surfaces of the **capacitor openings** , thus completely filling the bit line contact hole with the first polysilicon layer; removing portions of the conductive layer from the **top surface** of the second

insulator layer, to form storage node structures in the **capacitor openings** , and to form an upper level, bit line contact structure in the bit line contact...

...and in the capacitor dielectric layer, to form a bit line opening to expose the **top surface** of the upper level bit line contact structure, and to define capacitor structures (29) consisting...

Technology Focus:

... doped in situ during deposition via the addition of arsine, phosphine, to a silane. The **capacitor openings** and the bit line contact hole are formed via an anisotropic reactive ion etching (RIE...

...structure are defined via removal of HSG layer and of first polysilicon layer from the **top surface** of the second insulator layer via a chemical mechanical polishing. The second polysilicon layer is...

10/5,K/8 (Item 5 from file: 350)

013869479 **Image available**

WPI Acc No: 2001-353691/200137
Related WPI Acc No: 2000-022083; 2001-475491; 2002-224857; 2002-402181
XRAM Acc No: C01-109537
XRPX Acc No: N01-256838

Fabrication of capacitor for dynamic random access memory cell, involves depositing first layer, patterned polysilicon masking layer, and second layer over node location, and forming capacitor storage node

Patent Assignee: MICRON TECHNOLOGY INC (MICR-N)
Inventor: PAREKH K R; ZAHURAK J K

Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6228710	B1	20010508	US 97798879	A	19970211	200137	B
			US 99291423	A	19990413		

Priority Applications (No Type Date): US 97798879 A 19970211; US 99291423 A 19990413
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6228710	B1		33	H01L-021/8242	Cont of application US 97798879 Cont of patent US 5981333

Abstract (Basic): US 6228710 B1

NOVELTY - A capacitor is fabricated by sequentially forming a first layer, a patterned polysilicon masking layer, and second layer over a node location. The polysilicon layer is electrically connected to the node location to form a storage node. Dielectric and cell plate layers are coupled to the storage node. The dielectric layer, cell plate layer, and storage node together comprise the capacitor.

DETAILED DESCRIPTION - Fabrication of a capacitor involves forming a first layer (34) over a node location (25, 27, 29). A patterned polysilicon masking layer is formed over a portion of the first layer to form a masked portion and an unmasked portion. The unmasked portion overlies the node location. A part of the unmasked portion is removed to form a first opening having a base above the node location. A second layer is formed within the first opening and over the patterned polysilicon layer. The second layer does not completely fills the first opening, thus narrowing an internal dimension of the first opening. A second opening is formed which extends from the bottom of the first opening to the node location. It comprises an internal dimension equal to the narrowed internal dimension of the first opening. The two openings comprise a **capacitor opening** . The second layer is anisotropically etched to remove the second layer from the polysilicon layer and to leave a second layer spacer (66) within the **capacitor opening** . The polysilicon layer is electrically connected to the node location to form a storage node (81c, 83c) comprising the polysilicon layer. A dielectric layer (92) is formed extending below the bottom of

the first opening and proximate the storage node. A cell plate layer (94) is formed proximate the dielectric layer. The dielectric layer, cell plate layer, and storage node together comprise the capacitor (100c, 102c) within the **capacitor opening** .

USE - The method is used for fabricating a capacitor useful for dynamic random access memory (DRAM) cell.

ADVANTAGE - The method provides a capacitor, which increases DRAM circuit density.

DESCRIPTION OF DRAWING(S) - The figure is a cross-sectional view of the semiconductor wafer fragment showing the fabrication of the capacitor.

Node location (25, 27, 29)
First layer (34)
Second layer spacer (66)
Storage node (81c, 83c)
Dielectric layer (92)
Cell plate layer (94)
Capacitor (100c, 102c)
pp; 33 DwgNo 25/25

Title Terms: FABRICATE; CAPACITOR; DYNAMIC; RANDOM; ACCESS; MEMORY; CELL; DEPOSIT; FIRST; LAYER; PATTERN; MASK; LAYER; SECOND; LAYER; NODE; LOCATE; FORMING; CAPACITOR; STORAGE; NODE
Derwent Class: L03; U11
International Patent Class (Main): H01L-021/8242
File Segment: CPI; EPI

Abstract (Basic):
... equal to the narrowed internal dimension of the first opening. The two openings comprise a **capacitor opening** . The second layer is anisotropically etched to remove the second layer from the polysilicon layer and to leave a second layer spacer (66) within the **capacitor opening** . The polysilicon layer is electrically connected to the node location to form a storage node...

...layer, cell plate layer, and storage node together comprise the capacitor (100c, 102c) within the **capacitor opening** .

Technology Focus:
... node location comprises a diffusion region in the semiconductor substrate. The polysilicon layer comprises a **bottom surface** , and the second layer spacer comprises an **upper surface** . The polysilicon masking layer may be doped with a conductivity enhancing dopant...

10/5,K/15 (Item 12 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013145037 **Image available**
WPI Acc No: 2000-316909/200027
Related WPI Acc No: 2001-031134
XRAM Acc No: C00-095776
XRPX Acc No: N00-237871
Capacitor for dynamic random access memory circuits comprises substrate node location, insulative material layer, capacitor opening , **conductive material, protuberant structure, capacitor dielectric layer, and capacitor plate structures**
Patent Assignee: MICRON TECHNOLOGY INC (MICR-N)
Inventor: FAZAN P C; FIGURA T A; GRAETTINGER T M; LI L; MCCANLESS W H; PAREKH K R; SCHUELE P J; WU Z
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6049101	A	20000411	US 97880356	A	19970623	200027	B
			US 9836702	A	19980306		

Priority Applications (No Type Date): US 97880356 A 19970623; US 9836702 A 19980306
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6049101	A		13	H01L-027/108	Div ex application US 97880356

Abstract (Basic): US 6049101 A

NOVELTY - A capacitor comprises substrate node location (17), insulative material layer (34), **capacitor opening** , conductive material (40a), protuberant structure, capacitor dielectric layer (58b), and capacitor plate structures (56, 60b).

DETAILED DESCRIPTION - The capacitor comprises a substrate node location; an insulative material layer disposed on the node location; an **capacitor opening** through the layer; a conductive material disposed within the opening and in electrical connection with the node location, the conductive material almost fill the **capacitor opening** and has an **upper surface** ; a protuberant structure with insulative material, having portion(s) extending elevationally below and outwardly from the **upper surface** ; a capacitor plate structure disposed within the **capacitor opening** and on the protuberant structure portion; a capacitor dielectric layer disposed adjacent the capacitor plate structure; and a second capacitor plate structure disposed adjacent the capacitor dielectric layer.

USE - For dynamic random access memory (DRAM) circuits.

ADVANTAGE - Surface area available for accommodating or supporting storage capacitors are increased.

DESCRIPTION OF DRAWING(S) - The figure shows the processing step of the wafer fragment.

Node location (17)
Insulative layer (34)
Conductive material (40a)
Tubular projection(51) Inside surface (48a)
First capacitor structure(58b) Dielectric layer (56)
Second capacitor structure (60b)
pp; 13 DwgNo 16/16

Title Terms: CAPACITOR; DYNAMIC; RANDOM; ACCESS; MEMORY; CIRCUIT; COMPRISE; SUBSTRATE; NODE; LOCATE; INSULATE; MATERIAL; LAYER; CAPACITOR; OPEN; CONDUCTING; MATERIAL; PROTUBERANCE; STRUCTURE; CAPACITOR; DIELECTRIC; LAYER; CAPACITOR; PLATE; STRUCTURE

Derwent Class: L03; U11; U12; U13; U14

International Patent Class (Main): H01L-027/108

International Patent Class (Additional): H01L-027/108

File Segment: CPI; EPI

Capacitor for dynamic random access memory circuits comprises substrate node location, insulative material layer, capacitor opening , **conductive material, protuberant structure, capacitor dielectric layer, and capacitor plate structures**

Abstract (Basic):

... A capacitor comprises substrate node location (17), insulative material layer (34), **capacitor opening** , conductive material (40a), protuberant structure, capacitor dielectric layer (58b), and capacitor plate structures (56, 60b).

... comprises a substrate node location; an insulative material layer disposed on the node location; an **capacitor opening** through the layer; a conductive material disposed within the opening and in electrical connection with the node location, the conductive material almost fill the **capacitor opening** and has an **upper surface** ; a protuberant structure with insulative material, having portion(s) extending elevationally below and outwardly from the **upper surface** ; a capacitor plate structure disposed within the **capacitor opening** and on the protuberant structure portion; a capacitor dielectric layer disposed adjacent the capacitor plate...

Technology Focus:

... an interior surface (51) with a portion supporting the capacitor plate structure. The conductive material **upper surface** is planar.

10/5,K/16 (Item 13 from file: 350)

012953897 **Image available**
WPI Acc No: 2000-125747/200011
XRAM Acc No: C00-038206
XRPX Acc No: N00-094754

Capacitor structure fabrication process used to create a dynamic random access memory (DRAM) device with an increased surface area

Patent Assignee: TAIWAN SEMICONDUCTOR MFG CO (TASE-N)
Inventor: HSIAO Y; WANG C
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6004857	A	19991221	US 98154846	A	19980917	200011	B

Priority Applications (No Type Date): US 98154846 A 19980917
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6004857	A		11	H01L-021/70	

Abstract (Basic): US 6004857 A

NOVELTY - A dynamic random access memory (DRAM) capacitor is formed using a rough storage node structure resulting from the oxidation of tungsten silicide layer followed by the removal of the oxide layer from the bottom of unoxidized tungsten silicide layer.

DETAILED DESCRIPTION - A method for creating a capacitor structure for DRAM devices comprising the steps of:

(a) providing a transfer gate transistor comprising a polysilicon gate structure on a gate insulator layer (2) with a source/drain region not covered by the polysilicon gate structure;

(b) forming a storage node contact hole in composite insulator layer and exposing the **top surface** of source region of the source/drain region;

(c) forming a doped polysilicon plug (11) in the storage node contact hole contacting the source region;

(d) depositing a thick insulator layer;

(e) forming a **capacitor opening** in the thick insulator layer and exposing the **top surface** of the doped polysilicon plug (11);

(f) depositing a first polysilicon layer on the **top surface** of the thick insulator layer and exposed in the **capacitor opening** ;

(g) depositing a metal silicide layer on the first polysilicon layer (3);

(h) oxidation process to create an oxide layer consuming the top of the metal silicide layer with oxide layer overlying a bottom portion of unoxidized metal silicide layer;

(i) removing oxide layer from the **top surface** of the bottom portion of the unoxidized metal silicide layer;

(j) removing the second polysilicon layer (3), the bottom portion of unoxidized metal silicide layer, and the first polysilicon layer from the **top surface** of the thick insulator layer to create a storage node structure (19) in the **capacitor opening** ;

(k) removing the thick insulator layer from the **top surface** of the composite insulator layer (8);

(l) forming a capacitor dielectric layer (20) on the storage node structure; and

(m) forming a polysilicon upper electrode structure on the capacitor dielectric layer (20).

USE - The method is used for the fabrication of a DRAM capacitor structure having an increased surface area.

ADVANTAGE - DRAM capacitor has an increased surface area, thus providing greater storage capacity.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of a DRAM structure.

Semiconductor substrate (1)
Gate insulator (2)
Polysilicon layer (3)
Insulator layer (4)
Silicon oxide layer (8)
Doped polysilicon plug (11)
Storage node structure (19)

Capacitor dielectric layer (20)
ONO layer (21)
DRAM capacitor structure (23)
pp; 11 DwgNo 10/10
Title Terms: CAPACITOR; STRUCTURE; FABRICATE; PROCESS; DYNAMIC; RANDOM; ACCESS; MEMORY; DRAM; DEVICE; INCREASE; SURFACE; AREA
Derwent Class: L03; U11; U12; U13; U14
International Patent Class (Main): H01L-021/70
File Segment: CPI; EPI

Abstract (Basic):
... b) forming a storage node contact hole in composite insulator layer and exposing the **top surface** of source region of the source/drain region...

...e) forming a **capacitor opening** in the thick insulator layer and exposing the **top surface** of the doped polysilicon plug (11...

...f) depositing a first polysilicon layer on the **top surface** of the thick insulator layer and exposed in the **capacitor opening** ; (...

...i) removing oxide layer from the **top surface** of the bottom portion of the unoxidized metal silicide layer...

...the bottom portion of unoxidized metal silicide layer, and the first polysilicon layer from the **top surface** of the thick insulator layer to create a storage node structure (19) in the **capacitor opening** ; (...

...k) removing the thick insulator layer from the **top surface** of the composite insulator layer (8
?

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DATE: Friday, November 15, 2002 Printable Copy Create Case

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DB=TDBD; PLUR=YES; OP=OR			
L17	L16	4	L17
L16	L15 not l10	4	L16
L15	l8 and l3	8	L15
L14	l3 and l3	262	L14
L13	l9 and l3	4	L13
L12	L9 and (pga or lga or ppa or cpga or bga)	0	L12
L11	L10 not l7	0	L11
L10	L9 and l3	4	L10
L9	L8 and l5	462	L9
L8	L4 and capacit$	1721	L8
L7	L6 and capacit$	4	L7
L6	l3 and l4 and l5	30	L6
L5	semi adj conductor? Or semiconductor$ Or wafer$ Or ic or ics or integrated adj circuit? Or silicon near3 substrat$	9797	L5
L4	S apertur? Or orifice or opening? Or hole or holes Or gap or gaps or space? Or cavit$ Or notch? or window?	21331	L4
L3	(top or upper or lower or bottom)near2 surface?	262	L3
L2	(windowframe? Or window adj fram?)near3 capacitor?	0	L2
DB=USPT; PLUR=YES; OP=OR			
L1	(windowframe? Or window adj fram?)near3 capacitor?	0	L1

END OF SEARCH HISTORY

L17: Entry 3 of 4 File: TDBD Sep 1, 1973

TDB-ACC-NO: NN73091342

DISCLOSURE TITLE: Capacitively Driven Sectioned Tablet. September 1973.

PUBLICATION-DATA:
IBM Technical Disclosure Bulletin, September 1973, US

VOLUME NUMBER: 16
ISSUE NUMBER: 4
PAGE NUMBER: 1342 - 1347

PUBLICATION-DATE: September 1, 1973 (19730901)

CROSS REFERENCE: 0018-8689-16-4-1342

DISCLOSURE TEXT:

6p. In the single direction position transducing arrangement shown in Fig. 1, conductive grid lines or strips 1'-15' are shown conductively connected to the respective capacitor plates 21'-35'. Plates 21'-35' are of the same material as and integral with the conductive grid lines, so the grid lines widen at the ends into capacitive coupling pads. Position sensing in Fig. 1 is in the X-direction. Between each respective plate 21'-35' and triangular plate 17' beneath these plates there is a layer of dielectric. Thus plates 21'-35' are capacitively coupled to plate 17' to provide an array of capacitances 16'. The cutaway portions of plates 33' to 35' show dielectric at 32' and 34'. - Also capacitively coupled to each of the grid lines 1'-15' is plate 19', acting to provide a fixed capacitance voltage division path to ground for each grid line with the grid lines, acting as voltage taps for the divided voltage. Between each of the grid lines 1'-15' and plate 19' is dielectric shown at 12' and 14', of uniform thickness across the array. - In Fig. 1, the area of the respective capacitance plates of the array of capacitances 16' increases in size in the X-direction. When plate 17' is energized by AC source 18, voltage appearing on respective grid lines 1,-15,, increases in the same direction. Voltage changes as a function of position in the X-direction because of the geometry of plate 17'. With each plate 21'-35' of equal width and equally spaced in the X-direction, the output voltage sensed on grid lines 1'-15' changes from grid line to grid line. - Fig. 2 is an exploded view of a capacitive voltage divider arrangement for sensing position in both the X and Y directions, as indicated by the arrows adjacent plates 7 and 46, respectively. Instead of the single triangular X-drive plate shown in Fig. 1 at 17', there are shown complementary pairs of triangular drive plates including complementary X-drive plates 5 and 7 in the lower part of Fig. 2, and a complementary pair of X-drive plates, 9 and 10. The second complementary pair of plates insure high reliability in position sensing, balance and symmetry. If any X-direction grid line 11-25 breaks, both segments of the broken grid line continue to provide a voltage for sensing position. Drive plates 9 and 10 are voltage driven simultaneously with plates 5 and 7. Complementary pair X-drive plates 5-7 and 9-10 act, respectively, with capacitor plates 51, 53, etc. and 71, 73, etc., to capacitively couple, in varying amounts, the transducer drive signal from AC source 18 to X-direction sensing grid lines 11-25 via an interposed dielectric medium, not shown. - There is a set of complementary pairs of Y-drive plates, 46-47 and 48-49 which function in the same manner for voltage sensing in the Y-direction. - The transducer tablet is fabricated by depositing the X-grid lines 11-25 with their corresponding capacitor plates 51,53,71,73, etc. and Y-drive plates 46-49 on one side of a dielectric sheet, and the Y-grid lines 31-45 with their corresponding capacitor end plates and X-drive plates

5, 7, 9 and 10 on the other side of the sheet. Capacitors 50 and 52, shown in dotted line form in Fig. 2, represent the respective capacitances between plates 51 and 53 and the respective sections 55 and 57 of complementary plates 5 and 7. - In Fig. 3 a timing arrangement shows how driving plates of Fig. 2 are driven in time. Source 18 drives plates 5 and 7. During the X-drive time interval plates 9 and 10 are to be driven in the same manner, with X-drive plate 10 being driven simultaneously with X-drive plate 7 during a first subinterval of the X-drive time interval and then, with all X-drive plates 5, 7, 9 and 10 being driven simultaneously during the remainder of the X-drive time interval. During the Y-drive time interval, Y-drive plates 46 and 48 are first driven and then all y-drive plates 46, 47, 48 and 49 are simultaneously driven. - Fig. 3a shows the X-drive signal. Fig. 3b shows the Y-drive signal. Fig. 3c shows intervals for switching of switches 59 and 61. For details see U. S. patent 3,593,115. - Fig. 4 shows a portion of the cross-sectional view of the X-Y position transducer arrangement of Fig. 2. The view may be taken, parallel to the Y-grid lines 31-45 shown in Fig. 2. Dielectric layer 1 is a sheet of MYLAR* of selected thickness and uniformity. On both the top and bottom surfaces of the dielectric layer 1 a conductive layer of copper is deposited. The layers of copper are etched to form the layers of X and Y grid lines, shown as 15-19 and 45, respectively, in Fig. 4. On top of each of the layers of X and Y grid lines is another layer of dielectric 14 and 16. Dielectric is provided between the grid lines, as at 81. - The drive plates of Fig. 2 are not shown in Fig. 4. They are fabricated in the same way X-drive plates are etched on the bottom surface of dielectric layer 1, along with the Y-grid lines. Y-drive plates are etched on the upper surface of dielectric layer 14 with X-grid lines. - When stylus 4 is positioned on or above the layer of dielectric 14, a voltage indicative of the X-Y position of the stylus is capacitively coupled to the stylus. Stylus 4 is a conventional ballpoint pen conductively coupled from its point to an output device. A writing medium is interposed between the pen and tablet surface for making hard copy, while the movement of the pen is electronically being sensed for information recognition and entry into a computer. - Fig. 5a shows a four plate 71, 72, 73, 74 drive plate structure 75 for a tablet having three capacitor sections A, B, and C. Fig. 5b shows complimentary triangular drive plates 5, 7 used in the conventional, analog only, tablet described above in juxtaposition to the plates of Fig. 5A. The triangular structure produces the linearly varying voltage amplitude gradient and the constant reference amplitude, as required. Each section in Fig. 5A achieves this same triangular plate arrangement, amplitude gradient and the constant reference amplitude, as required. Each section in Fig. 5A achieves this same triangular plate arrangement, by combining at least two adjacent ones of the four plates 71, 72, 73, 74 to form a completed triangle. - The various ways in which plates are combined to form sections are represented in Fig. 6a, which shows drive plate connections. Fig. 6B shows a table of connections for four sections A, B, C, D and five plates with N sections N+1 drive plates are needed. Except for the end plates 71, 74 which are already triangular, all interior triangles are formed from the sum of the two adjacent quadrilaterals 72, 73. Although the whole combination is not a triangle, that portion in the region of the active section gives the capacitive plate area needed for the required linear voltage gradient. Any number of sections can be driven this way by adding another quadrilateral drive plate 72 for each additional section required, i.e., D, E. F.... - The drivers must be designed to have two states: active and grounded. A high-impedance state is not required, because the condition of an inactive terminal being internal to an active section does not occur. - Fig. 7 shows one completed axis of a three section tablet A, B, C, and shows the relationship between the drive plates 71-74 (75) and 71a-74a (76) and the coupling tabs 77 at the ends of the grid lines. The symmetrical design causes the same signal to be applied to both ends of a grid line and is tolerant to lines with a break. - The selection of the one section to be driven is determined by the position of pen 4. Conditions switch the drive from one section to another as pen 4 moves between them. When pen 4 is brought to the tablet surface after having been out of range of the signal, it is necessary to establish the initial section to be driven. One way is to sequentially drive each set of sections 71-74, 71a-74a, in corresponding pairs, one after the other, until the section under pen 4 is located. - The tablet can also be driven in the conventional mode of Fig. 2, not divided into sections 71-74, etc. This can be done as shown in Fig. 8 by adding conventional triangular drive plates 5, 7. When plates 5, 7 are driven the tablet has reduced resolution, since resolvable positions of a section are spread over the entire tablet. This, is more than adequate to resolve the section over which pen 4 is located. Only one A/D conversion cycle is

required to locate the section 71-74 to be activated. - With the addition of triangular drive plates 5, 7 the resultant signal coupled to the grid lines by the section plates is reduced. When the section plates are driven the triangular plates are both at AC ground. This adds a uniform capacitance to ground for all grid lines. The effect of capacitance to ground is to attenuate the grid line signal, without distorting the relationship between the linear voltage gradient and the constant reference. - When pen 4 is moved over the tablet surface 14 without being in contact with the tablet or a document it is useful to have pen coordinates available, to control a nonstoring cursor on a cathode-ray tube (CRT) display. As pen height above surface 14 increases, the width of the nonlinear regions at section boundaries grows. This results in discontinuities in digital output when switching from one section to the next, if pen 4 is too high. Use of triangular plates 5, 7 to give position when pen 4 reaches that height eliminates discontinuities. When so used, digital output of the analog position is shifted in significance to represent higher order bits. Triangular plates 5, 7 can be truncated to match the compressed zero to full-scale range of sections 71-74 and the number of sections, so there is an exact correspondence between high-order bits obtained when driving conventionally or by section. - To achieve very high linearity, the error in area ratios of the drive plates caused by a second gap in the overlap region between sections must be compensated. Depending upon gap size and plate width this error can be a few tenths of a percent or larger. This error is eliminated by reducing the gap width in the overlap region. Fig. 9 shows the drive plate design which gives precise compensation of area ratios (fringing can also be compensated) for the two drive plate combinations, that occur in the low and high-overlap regions at each end of a section. By adding 1/2 gap width of area to the center drive plate, both the high end and low end combinations have the perfectly linear geometric plate ratios required. * Trademark of E. I. du Pont de Nemours & Co.

End of Result Set

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L17: Entry 4 of 4 File: TDBD Jan 1, 1967

TDB-ACC-NO: NN6701977

DISCLOSURE TITLE: Fabrication of Capacitors. January 1967.

PUBLICATION-DATA:
IBM Technical Disclosure Bulletin, January 1967, US

VOLUME NUMBER: 9
ISSUE NUMBER: 8
PAGE NUMBER: 977

PUBLICATION-DATE: January 1, 1967 (19670101)

CROSS REFERENCE: 0018-8689-9-8-977

DISCLOSURE TEXT:

1p. Capacitors are formed using a folded, metallized dielectric tape. - A, a thin, flexible dielectric tape 11, e.g., of ceramic, is provided on top and bottom surfaces with a plurality of spaced conductive strips 12. The latter are deposited, by evaporation with the aid of suitable masking, by silk screening and the like. - In B, tape 11 is folded such that strips 12 form a plurality of electrodes. These are laterally spaced apart by the continuous dielectric tape 11. The ends of strips 12 overlap a folding edge of tape 11. If desired, the laminate is coated with varnish or epoxy to provide encapsulation. The laminate is then pressed to retain its shape. Finally, pretinned copper compression clips 13 are clamped at each end and bonded to the ends of strips 12 to provide electrical terminals for connection to external circuitry.

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Set      Items   Description
S1      233024   SEMI()CONDUCTOR? OR SEMICONDUCTOR? OR WAFER? OR IC OR INTE-
             GRATED()CIRCUIT? OR SILICON(3N)SUBSTRAT?
S2      134145   (TOP OR UPPER OR LOWER OR BOTTOM)()SURFACE?
S3      787934   APERTUR? OR ORIFICE OR OPENING? OR HOLE? OR GAP? ? OR SPAC-
             E? OR CAVIT? OR NOTCH
S4           1   (WINDOWFRAME? OR WINDOW()FRAM?)(3N)CAPACITOR?
S5         406   S1(S)S2(S)S3(S)CAPACIT?
S6          25   S1(3N)S2(3N)S3(3N)CAPACIT?
S7          16   S1(2N)S2(2N)S3(2N)CAPACIT?
S8         919   CAPACIT?(N)(WINDOW? OR S3)
S9          11   S8(3N)S1
? show files
File 348:EUROPEAN PATENTS 1978-2002/Nov W01
         (c) 2002 European Patent Office
File 349:PCT FULLTEXT 1979-2002/UB=20021107,UT=20021031
         (c) 2002 WIPO/Univentio
?
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9/5,K/8 **(Item 8 from file: 348)**
DIALOG(R)File 348:EUROPEAN PATENTS

00280717
CAPACITANCE PRESSURE SENSOR.
KAPAZITIVER DRUCKFUHLER.
DETECTEUR DE PRESSION CAPACITIF.
PATENT ASSIGNEE:
ROSEMOUNT INC., (300581), 12001 Technology Drive, Eden Prairie, MN 55344, (US), (applicant designated states: DE;FR;GB;IT;SE)
INVENTOR:
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Cross, Rupert Edward Blount et al (42891), BOULT, WADE & TENNANT 27 Furnival Street, London EC4A 1PQ, (GB)
PATENT (CC, No, Kind, Date): EP 311612 A1 890419 (Basic)
EP 311612 A1 900926
EP 311612 B1 930324
WO 8707947 871230
APPLICATION (CC, No, Date): EP 87903800 870529; WO 87US1235 870529
PRIORITY (CC, No, Date): US 877281 860623
DESIGNATED STATES: DE; FR; GB; IT; SE
INTERNATIONAL PATENT CLASS: G01L-007/08; G01L-009/12;
CITED PATENTS (EP A): EP 97339 A; WO 8602486 A
CITED PATENTS (WO A): JP 60233863 A; US 4084438 A
CITED REFERENCES (EP A):
See also references of WO8707947;
NOTE:
No A-document published by EPO
LEGAL STATUS (Type, Pub Date, Kind, Text):

Application:	890419	A1	Published application (A1with Search Report ;A2without Search Report)
Examination:	890419	A1	Date of filing of request for examination: 881104
Search Report:	900926	A1	Drawing up of a supplementary European search report: 900808
Examination:	910529	A1	Date of despatch of first examination report: 910416
Change:	911106	A1	Representative (change)
Grant:	930324	B1	Granted patent
Oppn None:	940316	B1	No opposition filed

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	EPBBF1	1457
CLAIMS B	(German)	EPBBF1	1566
CLAIMS B	(French)	EPBBF1	1596
SPEC B	(English)	EPBBF1	5148
Total word count - document A			0
Total word count - document B			9767
Total word count - documents A + B			9767

...SPECIFICATION or first glass layer 20, so that the holes indicated at 23 will overlie the **capacitance cavities** 14 on the **wafer** 10. The dielectric disc 20 is then metalized on both sides to form a metal...
?

7/TI,PN,PD,AN,AD,AB,K/11 (Item 1 from file: 349)

DRAM CELL HAVING A CAPACITOR STRUCTURE FABRICATED PARTIALLY IN A CAVITY AND METHOD FOR OPERATING SAME

CELLULE DRAM DOTEE D'UNE STRUCTURE DE CONDENSATEUR PARTIELLEMENT FABRIQUEE DANS UNE CAVITE ET PROCEDE D'EXPLOITATION

Patent and Priority Information (Country, Number, Date):
Patent: WO 200261806 A2 20020808 (WO 0261806)
Application: WO 2002US846 20020111 (PCT/WO US0200846)

English Abstract
A memory system that includes a DRAM cell including an access transistor and a capacitor structure fabricated in a semiconductor substrate. The capacitor structure is fabricated by forming a cavity in a shallow trench isolation region, thereby exposing a sidewall portion of the substrate below the upper surface of the substrate. The capacitor structure is formed at least partially in the cavity, below the upper surface of the substrate. The capacitor structure extends over the sidewall portion of the substrate, thereby increasing the surface area of the capacitor structure, while minimizing the layout area of the capacitor structure. The memory system may include positive and/or negative boosted voltage generators coupled to a word line driver. The positive boosted voltage is less than one diode voltage drop greater than VDD. The negative boosted voltage is less than VSS by less than the absolute value of one diode voltage drop.

French Abstract
L'invention concerne un systeme de memoire qui comporte une cellule DRAM comprenant un transistor d'acces et une structure de condensateur fabriquee dans un substrat semi-conducteur. La structure de condensateur se fabrique en formant une cavite dans une region d'isolation par tranchees peu profondes, ce qui expose une partie de paroi laterale du substrat au-dessous de la surface superieure dudit substrat. La structure de condensateur est formee au moins partiellement dans la cavite, au-dessous de la surface superieure du substrat. Cette structure recouvre la partie laterale du substrat, ce qui augmente la surface active de la structure de condensateur, tout en reduisant la zone d'implantation de ladite structure. Le systeme de memoire peut comprendre des generateurs de tension augmentee positive et/ou negative couples a une commande de lignes de mots. La tension augmentee positive est inferieure a une chute de tension de diode superieure a V"sub"DD. La tension augmentee negative est inferieure a V"sub"SS d'une valeur inferieure a la valeur absolue d'une chute de tension de diode.

Fulltext Availability:
Claims

Claim
... upper surface of the semiconductor
substrate;
forming a cavity in the field dielectric, wherein the
cavity extends below the upper surface and exposes a sidewall
portion of the **semiconductor** substrate below the **upper surface** ;
and
forming the **capacitor** structure in the **cavity** , such that
the **capacitor** structure extends over the sidewall portion and
is at least partially recessed below the upper...

...a first conductivity type;
a field dielectric region located below an upper surface of
the **semiconductor** substrate and having a **cavity** located
therein, the **cavity** extending below the **upper surface** and
exposing a sidewall portion of the **semiconductor** substrate;
a **capacitor** structure in the **cavity** , such that the capacitor
structure extends over the sidewall portion and is at least
partially...
?